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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,126	01/16/2004	Bruce R. Ferguson	MSEMI.110A	7205

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EXAMINER	
PIGGUSH, AARON C	
ART UNIT	**PAPER NUMBER**
2838	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	12/22/2006	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 12/22/2006.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/760,126	FERGUSON, BRUCE R.	
	Examiner	Art Unit	
	Aaron Piggush	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 9-14 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 23-25 and 27-29 of copending Application No. 10/758952. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 23 and 24 of application 10/758952 disclose all of the limitations of claims 9 and 10 of the instant application, wherein the "transistor" of the instant application is met by the "bi-directional transistor" of application 10/758952 because a bi-directional transistor is still a transistor. Additionally, claims 25, 27, 28, and 29 of application 10/758,952 claim all of the limitations of claims 11, 12, 13, and 14, of the instant application, respectively.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-14, 16, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faberman (US 5,978,236) in view of Krall (US 5,621,299).

With respect to claims 9, 10, and 16, Faberman discloses a method for controlling battery power comprising the acts of: selectively providing a first external power source to a device coupled to a system power terminal ("AC power in" in Fig. 5); coupling an internal battery to the system power terminal via series-connected transistor (charge switch in Fig. 5 made up of no. D4F and S1F); charging the internal battery by regulating the transistor to conduct a charging current in a first direction from the system power terminal to a positive battery terminal during a charging mode (col 12 ln 7-22), wherein the charging current is linearly adjusted to limit the supply current (col 7 ln 65 to col 8 ln 41); and discharging the internal battery by regulating the transistor to conduct a discharging current in a second direction from the positive battery terminal to the system power terminal during a discharging mode (col 12 ln 18-35).

However, Faberman does not expressly disclose selectively providing a first or a second external power source to a device (i.e. wherein this is interpreted to mean that there are two separate external power sources which can be switched between), or adjusting the charging current to prevent a supply current from exceeding a predefined threshold.

Krall discloses selectively providing a first or a second external power source to a device (no. 27 and 29 in Fig. 1, including switches no. 14 and 16) and adjusting the charging current to prevent a supply current from exceeding a predefined threshold (no. 47 in Fig. 1, all components of Fig. 5, and col 6 ln 33-67), in order to prevent damage to the wiring or the batteries resulting from too great of a current or the heat generated therefrom.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to provide a selectable first or second external power source and adjust the charging current to keep it from exceeding a predefined threshold in the device of Faberman, as did the device of Krall, so that the batteries and wiring would not be damaged from too great of a current.

With respect to claim 11, Faberman discloses wherein the impedance of the transistor varies to limit the level of the charging current (col 7 ln 65 to col 8 ln 41 and col 12 ln 7-35). As the switch is turned on and off, the amount of charging current is limited to a certain amount. Furthermore, when the switch is off, its impedance is so high that current cannot flow through, and when it is on, the impedance is lowered so that a current may flow.

With respect to claim 12, Faberman discloses wherein the charging mode occurs when the voltage on the system power terminal is greater than the voltage of the internal battery (col 3 ln 42-60 and col 5 ln 5-25). This is further understood because when the AC power of the system is functioning correctly and supplying power to the system, it is used to charge the battery. Additionally, when there are two DC voltage sources (e.g. the battery and the rectified input power from the AC source), current flows from the source of the higher potential to the source of the lower potential, as is well-known to one of ordinary skill in the art.

With respect to claim 13, Faberman discloses wherein the discharging mode occurs when the voltage on the system power terminal is less than the voltage of the internal battery (col 3 ln 42-60 and col 5 ln 5-25). This is further understood because when the AC power of the system is functioning incorrectly or is turned off and not supplying power to the system, the battery must be used to power the system. Additionally, when there are two DC voltage sources (e.g. the battery and the rectified input power from the AC source), current flows from the source of the higher potential to the source of the lower potential, as is well-known to one of ordinary skill in the art.

With respect to claim 14, Faberman discloses wherein the discharging mode occurs in response to a discharge command col 3 ln 42-60 and col 19 ln 1-34). When the main power supply (i.e. AC power in) is lost by a power outage or other type of unintentional failure, there is an automatic command wherein the battery will supply power to the device.

With respect to claim 18, Faberman discloses charging the internal battery by regulating the transistor to conduct a charging current in a first direction from the system power terminal to a positive battery terminal during a charging mode (col 12 ln 7-22), wherein the charging current is linearly adjusted to limit the supply current (col 7 ln 65 to col 8 ln 41); and discharging the internal battery by regulating the transistor to conduct a discharging current in a second direction from the positive battery terminal to the system power terminal during a discharging mode (col 12 ln 18-35).

However, he does not disclose sensing a supply current from the second external power source, or adjusting the charging current (overriding the driving signal) to reduce the transistor's current level when the current sense signal exceeds the threshold value.

Krall discloses selectively providing a first or a second external power source to a device (no. 27 and 29 in Fig. 1, including switches no. 14 and 16), sensing a supply current from the second external power source (no. 47 in Fig. 1, all components of Fig. 5, and col 6 ln 33-67), and adjusting the charging current (overriding the driving signal) to reduce the transistor's current level when the current sense signal exceeds the threshold value (no. 47 in Fig. 1, all components of Fig. 5, and col 6 ln 33-67), in order to prevent damage to the wiring or the batteries resulting from too great of a current or the heat generated therefrom.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to sense a supply current from the power source and adjust the charging current level when the current sense signal exceeds the threshold value in the device of Faberman, as did the device of Krall, so that the batteries and wiring would not be damaged from too great of a current.

With respect to claims 19 and 20, Faberman discloses wherein the transistor is a MOSFET (or field effect transistor) with a configurable body contact (no. S1F in Fig. 5, similar to S6H in Fig. 6, can be a MOSFET [i.e. obvious and well known that a MOSFET acts as a switch, and Faberman uses MOSFETs as switches throughout his circuit], wherein the MOSFET can conduct in both directions (col 13 ln 38-59)).

Although Faberman does not expressly disclose wherein the MOSFET is a P-channel MOSFET, it is implied that the MOSFET could be a P-channel or N-channel MOSFET (as both were well known at the time of the invention). Furthermore, it would have been obvious to use a P-channel MOSFET due to circuit simplification in medium and low power applications (versus an N-channel MOSFET). Furthermore, it would be beneficial to configure/connect it as the

enhancement mode MOSFET because it would be less subject to random static charges (i.e. greater protection).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a P-channel MOSFET as the MOSFET switch in the device of Faberman, so that the circuit could be simplified (at least with medium and low power applications), which would lead to reduced manufacturing costs.

With respect to claim 21, Faberman does not expressly disclose automatically disconnecting an external secondary power source when the external primary power source is connected.

Krall discloses automatically disconnecting an external secondary power source when the external primary power source is connected (col 3 ln 59-67 and no. 14 and 16 in Fig. 1), in order to avoid any external or internal circuit complications (i.e. damage to the power source or the device itself) from having two different power sources connected at the same time.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to disconnect the secondary power source when the primary source was connected in the device of Faberman, as did Krall, so that damage to the power source or the device itself could be avoided (from having two different power sources connected at the same time).

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Faberman (US 5,978,236) and Krall (US 5,621,299), and further in view of Henrie (US 6,170,062).

With respect to claim 17, Faberman discloses wherein the external primary power source is an AC adapter ("AC power in" in Fig. 5), however, does not expressly disclose wherein

another external power source is a USB power interface (although he does disclose supplying power to other components by use of a USB in col 20 ln 8-20).

Henrie discloses a dual power supply on a USB system wherein a secondary external power source is a USB power interface (abstract, Fig. 9b, and col 2 ln 48-67), in order to provide a dual means of communication and power supply for various computer components.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include a USB power interface as the secondary external power source in the device of Faberman, as did Henrie, in order to provide greater compatibility with various power sources available at different locations in which the device may be used, along with providing a port that could also be used to communicate with another device.

Response to Arguments

6. Applicant's arguments filed August 7, 2006 have been fully considered but they are not persuasive.

With respect to claim 9, applicant argues that Faberman does not disclose, teach, or suggest linearly adjusting a charging current conducted by a transistor to the battery.

Examiner respectfully disagrees for the following reasons: Faberman does disclose linearly adjusting a charging current conducted by a transistor to the battery (as noted in the rejection above and further explained below), which is similar to the use of a bi-directional transistor as used in the applicant's invention wherein the applicant's transistor is controlled by the pass element driver (i.e. the applicant is also using a transistor to linearly adjust the charging current). Faberman's transistor/switch (number S1F in Fig. 5 [similar to S6H in Fig. 6] can be a MOSFET (i.e. obvious and well known that a MOSFET acts as a switch, and Faberman uses

MOSFETs as switches throughout his circuit), wherein the MOSFET can conduct in both directions (col 13 ln 38-59)) can reasonably be considered to be linearly regulating the charging current during the time periods when it is on. Furthermore, the duty cycle could be set to 1 for certain time periods which would also meet the applicant's claim language.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron Piggush whose telephone number is 571-272-5978. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AP

KARL EASTHOM
SUPERVISORY PATENT EXAMINER